

**FERROELECTRIC MEMORY DEVICES WITH IMPROVED
FERROELECTRIC PROPERTIES AND ASSOCIATED METHODS FOR
FABRICATING SUCH MEMORY DEVICES**

Abstract of the Disclosure

5 Pursuant to embodiments of the present invention, ferroelectric memory devices are provided which comprise a transistor that is provided on an active region in a semiconductor substrate, and a capacitor that has a bottom electrode, a capacitor-ferroelectric layer and a top electrode. These devices may further include at least one planarizing layer that is adjacent to the side surfaces of the bottom electrode such that
10 the top surface of the planarizing layer(s) and the top surface of the bottom electrode form a planar surface. The capacitor-ferroelectric may be formed on this planar surface. The device may also include a plug that electrically connects the bottom electrode to a source-drain region of the transistor. The ferroelectric memory devices according to embodiments of the present invention may reduce ferroelectric
15 degradation of the capacitor.